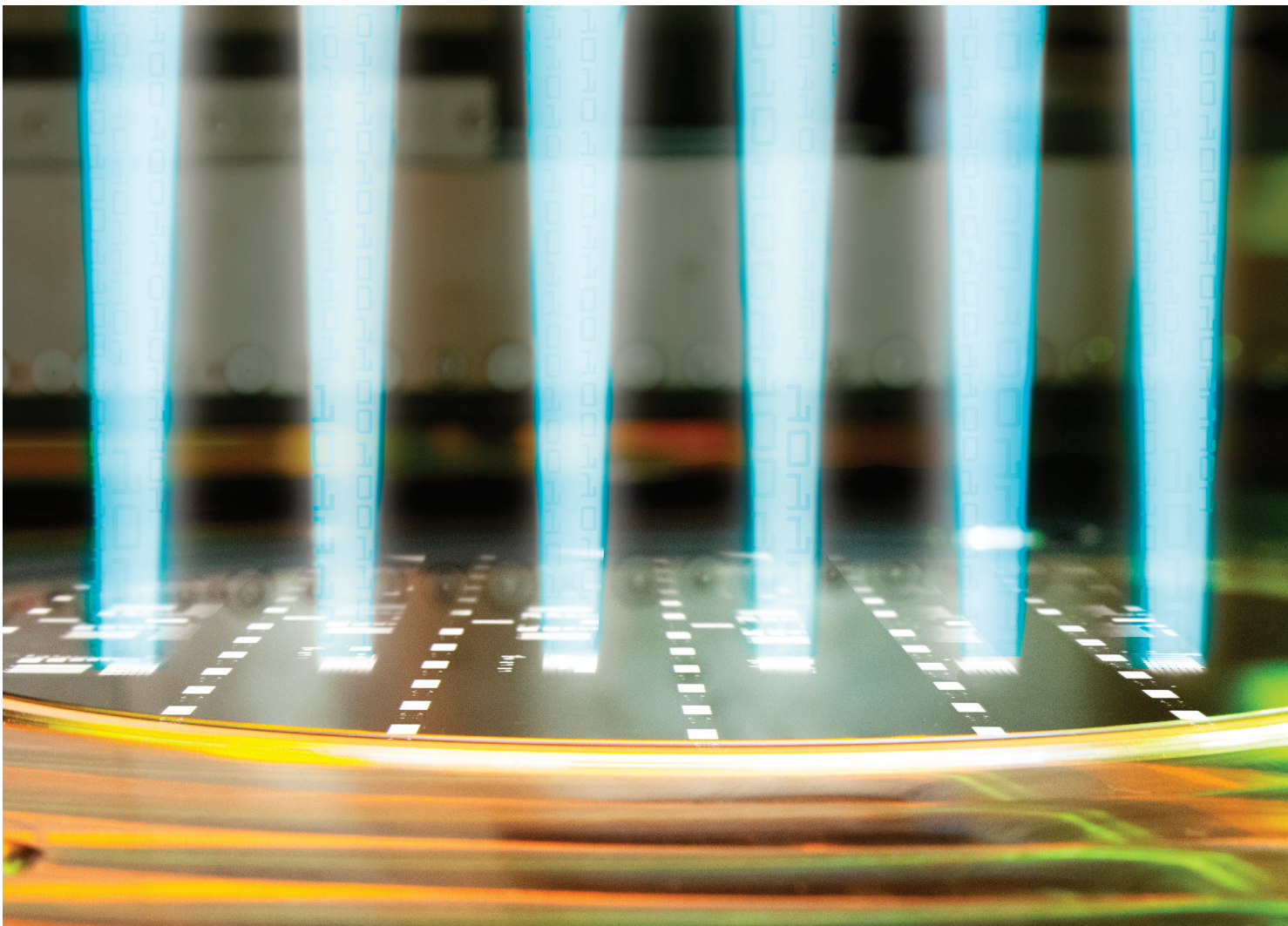


EV GROUP® | Technologies

MLE™ Maskless Exposure



Maskless Exposure Technology

Beyond traditional mask-based, toward digital lithography technology

Introduction

New demands on electronic device performance and flexibility are transforming the manufacturing infrastructure away from traditional mask-based lithography and toward digital lithography for advanced packaging and heterogeneous integration. Systems on chip are moving away from monolithic solutions toward modular systems in package, chiplets and functional blocks. Consequently, demand is growing for scalable and versatile back-end lithography to enable interconnection on the package and system level. New tools for mass production that can swiftly integrate novel functional elements via advanced packaging are required to meet this new industry vision. The high-volume-manufacturing (HVM) industry must reach beyond conservative chip patterning and enter into the new era of digital lithography technology.

EV Group has developed MLE™ (Maskless Exposure) technology to meet the critical requirements of design flexibility and minimal development cycles in the HVM world by eliminating mask-related difficulties and costs. MLE™ resolves the disruption between versatile (but slow) development machinery and fast (but inflexible) production. It provides a scalable solution that simultaneously enables die- and wafer-level design, supports established and new materials, and delivers high-speed adaptability at high reliability with multi-level redundancy for greater yield and lower cost of ownership (CoO).

EVG's MLE™ technology meets the critical requirements for back-end lithography not only in advanced packaging, but also for MEMS, biomedicine and printed circuit board manufacturing.

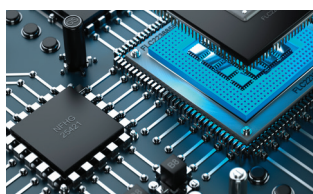
Key Aspects

- Full-resolution, stitch-free dynamic photoresist patterning
- Better than 2 µm line / space resolution in any arbitrary direction
- Design freedom & data confidentiality thanks to digital programmable layouts
- Individual die annotations (serial numbers, encryption keys, etc.)
- Compensation of wafer-level adaptive registration
- Unaffected by substrate deformation and warpage (thick wafers, glass or organic substrates)
- Smart & agile digital lithography processing infrastructure
- Consumables-free technology

Back-end lithography for advanced packaging faces new challenges

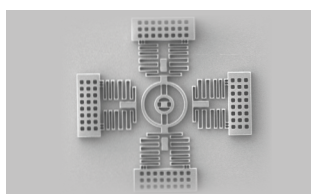
As heterogeneous integration becomes an increasing driving force in semiconductor development and innovation, impacting the advanced packaging, MEMS and PCB markets, back-end lithography requirements are growing. In advanced packaging, for example, the minimum resolution requirements for redistribution layers (RDL) and interposers with their continuously denser lines/spaces (L/S) are becoming increasingly stringent. In some cases, they are approaching or exceeding two microns, while die placement variation and the use of cost-efficient organic substrates require more flexibility in patterning. The requirements for higher overlay accuracy as well as high depth of focus in vertical sidewall patterning are also growing. New requirements, such as minimizing pattern distortion and die shift due to wafer distortion in fan-out wafer level packaging (FoWLP) and support for thick and thin resists, are just some of the criteria for existing and future advanced packaging lithography systems.

Advanced Packaging



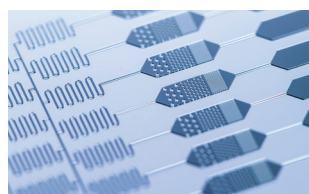
- Redistribution layer patterning for large size interposer, Fan-out & Fan-in WLP devices
- No reticle size restriction
- Variable patterning with distortion and die shift compensation
- High patterning throughput for low cost

MEMS



- High product mix and high mask / reticle cost drive need for maskless lithography
- 3D resist patterning for multi-step and slanted angle edge processes
- High depth of focus for patterning in trenches

Bio and Medical



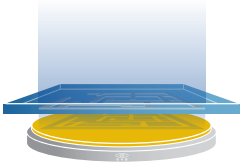
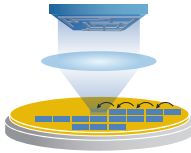
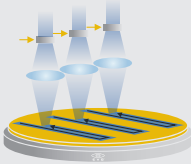
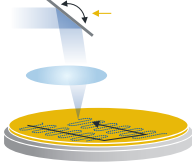
- Large size fluidic devices
- Pattern in the µm to mm range
- Ideal low cost of ownership
- Highly adaptable patterning solution for high product mix
- Scalable for various substrate sizes and biocompatible materials

HDI Printed Circuit Boards



- PCB line and space resolution needed for embedded die and high-density redistribution
- Warpage and die placement correction mandatory
- Variable patterning of multiple panel sizes

Exposure Principles Fundamentals

Exposure method	Proximity Mask Aligner	BEOL Projection Stepper	MLE™ Maskless Exposure Technology	Laser Direct Imaging
				
Exposure field size	Full field	Reticle Size limited (up to 50 mm x 25 mm)	Clustered Write Heads	Individual Laser Spots
Exposure wavelength	Broadband (g, h, i-line)	i-line/ Broadband	Multiple - Wavelength Exposure Optics	Single Wavelength
Resolution L/S	> 3 µm	> 1.5 µm	< 2 µm	Objective dependent down to 600 nm at very restricted throughput

Patterning Approaches

The core element of each lithography process is the exposure unit, which defines the characteristic performance of the lithography technology. Currently, there are several common exposure methods available on the market. In the case of mask aligners, the pattern is directly exposed onto a substrate through a mask, which is in close proximity to the photo-sensitive, resist-coated wafer. The minimum pattern size is defined by the exposure gap between the mask and wafer. Close proximity of the mask and resist surface will enable smaller patterns; however, too close a gap will cause mask contamination and lead to yield issues. Even though minimum resolution in production is limited to several microns, mask aligners are enabling solutions for low-cost, high-throughput patterning, especially when high exposure dose and thick photoresists or wafer-level designs are needed.

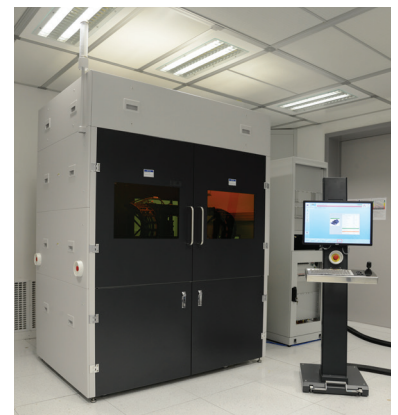
To overcome some of these process difficulties, back-end-of-line (BEOL) steppers use projection optics between a mask/reticle and wafer to pattern smaller feature sizes without contamination. However, the exposure occurs sequentially or step-wise with strong accelerations between exposures, as the optical design of the complex objectives and therefore the exposure field size are restricted.

Mask aligners as well as steppers are mask-based, where in addition to the aforementioned limitations, mask-related costs represent a significant additional cost factor to the overall patterning process. One solution to rule out mask cost is laser direct imaging technology, using individual or multiple laser beams that expose small geometrical elements in a sequential fashion. Even considering the advantages of direct imaging techniques, the sequential nature of the exposure results in considerable cost with very low throughput.

MLE™ technology exposes one or multiple wide strips in a parallel scanning fashion and accommodates any wafer size up to panels through a tightly integrated clustered write-head configuration. It supports all commercially available resists using a multi-wavelength high-power UV source. Throughput is independent of layout complexity and resolution, and MLE™ achieves the same patterning performance regardless of photoresist. MLE™ complements EVG's existing lithography systems, targeting new and emerging use cases where other approaches face scalability, CoO and other limitations.

Addressing novel lithography schemes

EVG's MLE™ technology pushes the boundaries of established lithography systems. MLE™ technology enables high-resolution (<2 microns L/S), stitch-free maskless exposure of the entire substrate surface with high throughput and low CoO. The system scales according to user needs by adding or removing UV exposure heads – for facilitating rapid transition from R&D to HVM mode, for throughput optimization, or for adaptation to different substrate sizes and materials – and is ideal for processing a range of substrates from small silicon or compound semiconductor wafers up to panel sizes. MLE™ achieves the same patterning performance regardless of photoresist thanks to a flexible and scalable high-power UV laser source, which provides multiple wavelength exposure options.



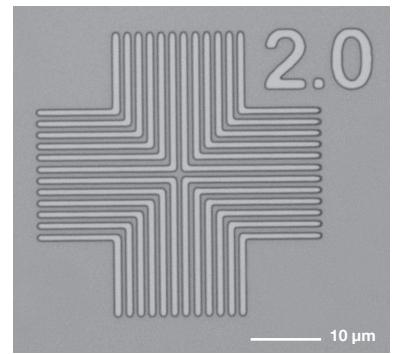
Unsurpassed flexibility, scalability and cost-of-ownership benefits compared to existing high-volume-manufacturing lithography methods

MLE™ technology eliminates the dilemma of continuously increasing mask costs for various chip designs and mask inventory management, which represent a significant part of overall development and production costs. Reducing the impact of pattern variability (in terms of substrate sizes and materials diversity) on time to market is another growing demand in back-end lithography. MLE™ technology is a scalable approach that allows patterning of any substrate shape, from various wafer sizes up to panels. The demo-ready technology employs clustered multi-wavelength laser light sources operating at 375 nm and/or 405 nm wavelengths, thus enabling thin resist patterning, including positive and negative resists, polyimides, dry film resists and PCB patterning, as well as thick resist exposures supporting high aspect ratios typically seen in wafer-level packaging, MEMS structuring, microfluidics and integrated silicon photonics applications.

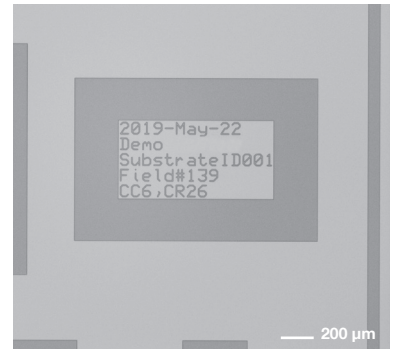
Besides mask-related difficulties, current mask-based technologies also face process issues related to high-order substrate deformations, and thus have limited control of distortions. In contrast, MLE™ technology is able to adapt to high substrate stress, bow and warp thanks to integrated dynamic alignment in order to adjust to substrate material and surface variation while actively compensating for mechanical die placement and stress-induced inaccuracies (such as rotation, shift, expansion and high order distortion errors). In parallel, it allows real-time digital/'binary' wafer-level-layout and individual-die-layout patterning simultaneously; in particular, ad hoc individual die annotation, serial number or encryption key implementation. Additionally, programmable modulations of UV dosage during the patterning process enables resist thickness level variation after the development process. This exceptional feature enables the fabrication of complex 3D multi-level resist patterns applicable in future MEMS, novel photonic devices or micro-optical elements (refractive, diffractive). The digital programmable die/wafer layout can be stored in numerous industry standard vector file formats (e.g. GDSII, Gerber, OASIS, ODB++, or BMP). The vector layout with any given pattern complexity is computationally processed (rasterized) within a few seconds and stored in bitmap format. As a result, neither resist type (pos./neg.), exposure dose level nor any given design layout complexity have any impact on the speed of the patterning process.

Toward a new digital infrastructure

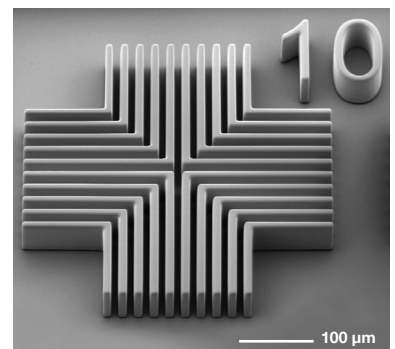
The aim of the novel MLE™ (maskless exposure) technology developed by EV Group is not only to bring a new lithography tool to the market, but also to address a trend toward smart and agile digital processing in the semiconductor industry while delivering unique maskless scalability in throughput, format and related consumables-free infrastructure. Utilizing this state-of-the-art exposure technology also tackles challenges faced by novel markets that are driven by the deployment of new materials or flexible substrates. The almost unlimited design flexibility that this novel technology brings to the current conservative environment opens up room for new innovations, helps to shorten development cycles, and at the same time bridges the gap between R&D and HVM by making exactly the same technology available to both fields. In the highly competitive global semiconductor industry market, manufacturing flexibility, scalability, development and operational costs are already extremely important factors for reducing time-to-market, which is essential to hold and expand market share by delivering similarly ground-breaking solutions to the end-customer. In summary, the new digital infrastructure enables dynamic device innovation while keeping costs at a reasonable level.



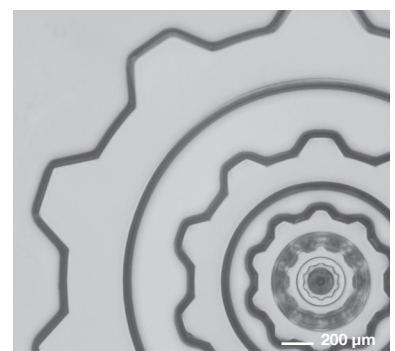
MLE™ exposure in high resolution AZ MIR 701 positive tone photoresist **Source: EVG**



Individual die annotation using MLE™ technology **Source: EVG**



MLE™ exposure in 50 µm thick layer JSR THB 151N negative tone resist **Source: EVG**



MLE™ exposure in 600 µm thick SU8 **Source: EVG**

