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Maskless Lithography Addresses Shift Toward 3D Integration

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Introduction

The continuous development and capability of lithographic patterning equipment for semiconductor manufacturing is driven by several megatrends, which are shaping our digital society. As 2D-IC density scaling is reaching its cost limits, especially for the patterning processes, advances in miniaturization and device performance are currently being extended toward 3D integration and heterogeneous integration (HI) within advanced packaging. This novel approach is seen as a key enabler for next-generation devices, where mobile processors have triggered a first growth cycle in 3D/HI. This growth cycle is expected to continue as high-performance applications such as artificial intelligence (AI) and 5G gain traction in mobile devices, but also due to other megatrends such as autonomous driving, which necessitates high reliability and data network capacity, as well as the Internet of Things (IoT).

Advanced packaging technologies have both increased in complexity as well as in number of options over the years. Transformation from single to multi-die packaging, enabled by 3D integration, is one example, which addresses the challenge of handling big data generated by high-performance computing. The continuous innovation of chiplet design and variety of integration schemes (on silicon, embedded or in package) can finally include several patterning levels. The increased importance of design flexibility and the ability to adopt both die and wafer-level designs simultaneously in back-end lithographic processing have to be addressed due to the need to shorten development cycles and cover the wide variety of advanced packaging platforms at the same time. In addition, any advanced product design mix adds to multiple masking levels, and correspondingly masks and mask inventory/cleanroom storage represent a high portion of overall production costs. Additionally, replacement costs for conventional laser sources or Hg lamps can add up to significant levels. The wait time for new physical mask sets as well as overall proof-of-new-design concepts for high product-mix designs intrinsically lead to prolonged development cycles for conventional mask-based production environments.

These requirements triggered the development of our maskless exposure (MLE™) technology to resolve critical needs in semiconductor packaging. MLE technology directly tackles this crucial demand for design flexibility while enabling unique scalability in both development and production facilities – thus shortening development cycles between R&D and production phase – by eliminating mask-related difficulties and consumables costs. The technology features high-resolution (<2 µm L/S), stitch-free, dynamically addressable exposure of the entire substrate surface, which enables agile processing and low cost of ownership (CoO).

Limitations of traditional exposure methods in back-end processing

Fundamentally, the resolution of any optical imaging system is determined by the ratio of exposure wavelength and its numerical aperture (NA). By definition, NA defines the light-gathering and light-emitting ability through the lens, and is characterized by the angle of aperture and thereby highly dependent on focal length. Technically, alteration of NA in exposure systems tends to be more cost effective than shortening the UV wavelength of the light source. Imaging exposure systems (such as steppers) are typically driven towards higher NA to enable structuring of finer critical dimensions. In contrast, higher NA reduces the depth of focus. Finding a compromise between resolution and focal depth is often a decisive parameter for the interconnect circuit design. This is especially true in advanced packaging as reconstitution of wafers is a central element in integrating die from various wafer manufacturers in a multi-die solution. Apart from those physical limitations, inaccuracies from die placement and die shift variations caused by over-molding add an additional layer of difficulty that current lithography steppers and other mask-based systems struggle to cope with. In addition, the given reticle size and optics dimensions of static exposure systems limit the exposure area. This can become particularly challenging for larger die interposer fabrication, where stitch lines or mismatched overlap regions of reticle exposure fields can affect electrical properties within the redistribution layer (RDL). The ability to generate a stitch-less pattern for interposers exceeding current reticles size is increasingly important for advanced devices with complex layouts needed for advanced graphics processing, AI and high-performance computing (HPC).

MLE addresses these needs through a combination of sub-nanometer range stage motion accuracy, distortion-free, high-intensity optics and real time patterning of a vector-based mask file. For reference, other approaches that need to rasterize the mask image prior to patterning, generate in the range of 141GB of data for every 300 mm wafer. Finally, the digital mask pattern is projected with sub-µs timing accuracy onto the substrate surface. Like most modern lenses, the MLE imaging system is diffraction-limited, and it supports a depth of focus (DoF) of +- 12 µm. A measurement of the DoF process window performance at 2 µm L/S together with the simulated curve is displayed below in Figure 1.

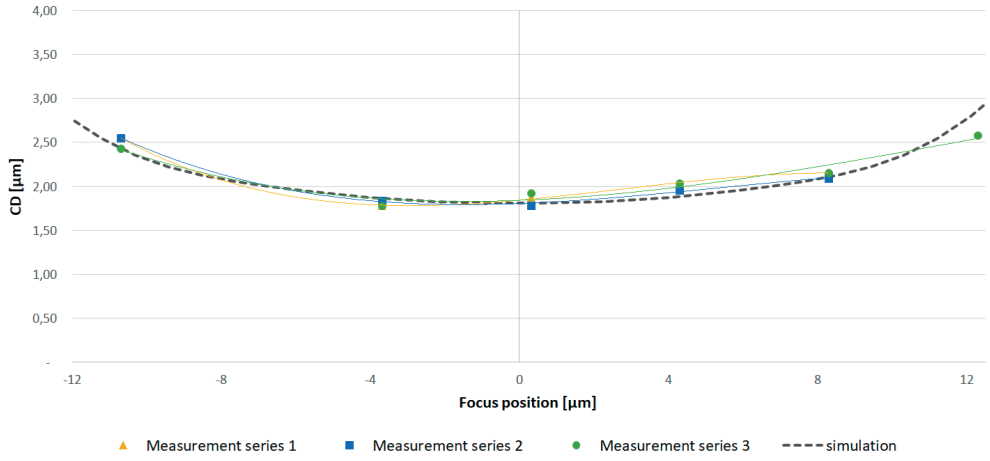

Figure 1
Critical dimension versus focus position for DoF process window evaluation

On top of the exposure window, the relatively small exposure field and the < 1 µm precise autofocus extends the usable dynamic focused range to more than 100 µm. The ability to control the focus position on a larger scale of the wafer position via chuck positioning and wafer clamping enables compensation for bowed and warped substrates.

Dynamic exposure methods and active die-shift compensation

Current back-end lithographic systems have no control over distortions smaller than the exposure field and therefore face difficulties with non-linear, high-order substrate distortions and die-shift-related issues, especially after die reconstitution on the wafer. MLE employs dynamic alignment modes with an automatic focus, in order to adapt to the substrate material and surface variations. The advanced distortion functionality relates and analyzes real-time data from synchronized visible or near-infrared topside and backside alignment. It accomplishes this by actively compensating for mechanical die placement, stress-induced inaccuracies such as rotation, displacement, expansion and high-order distortions of the substrate. The process flow of the advanced distortion correction function and dynamic alignment modes are visualized in Figure 2. Dynamic alignment includes both global as well as multi-point wafer alignment options, where typically up to 16 alignment marks (marked with blue and yellow), can be placed randomly in the layout in order to comprehensively cover the most critical areas on the substrate and compensate for global distortions. After misalignment measurement, displacement vectors are further compiled in parallel before the design is interpolated and rendered in real-time. The exposed patterns are therefore fully error compensated without inducing overlapping or non-covered regions – delivering minimum misalignment with no impact to the throughput of the patterning process. A visualization of a compensated layout (dark-grey) after an extreme atypical misalignment (indicated with red arrows) example is shown as a result after compensating the actual position of 16 marks (yellow) of multi-point alignment through the dynamic alignment mode.

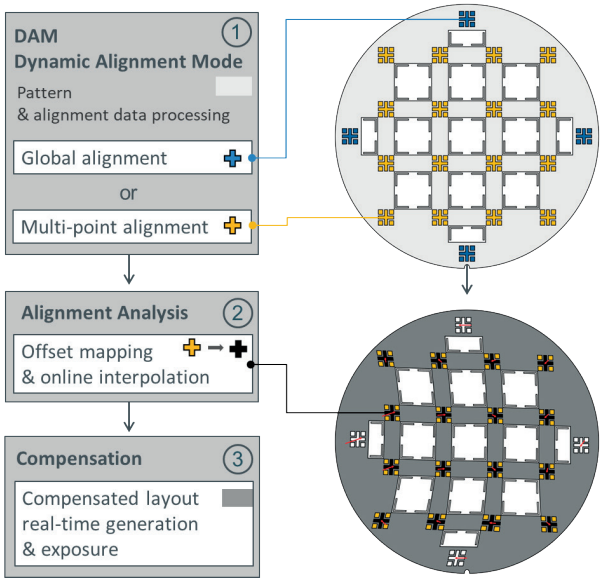

Figure 2
Advanced distortion compensation schematic process flow

Backside alignment plays a substantial role when it comes to bonded, opaque substrates or non-transparent materials used in multi-layer and multi-die processing. Referencing to the same structure for multiple exposures also helps to minimize misalignment as current pattern design density increases. Overlay errors or misalignment of any kind impact the electrical properties of contacts and insulation, and might create connection failures that significantly affect fab yield, overall productivity and CoO. Systems equipped with MLE technology integrate full wafer backside alignment (see Figure 3) utilizing dedicated objectives with near IR capability and proprietary chuck design accommodating wafer sizes up to 300 mm.

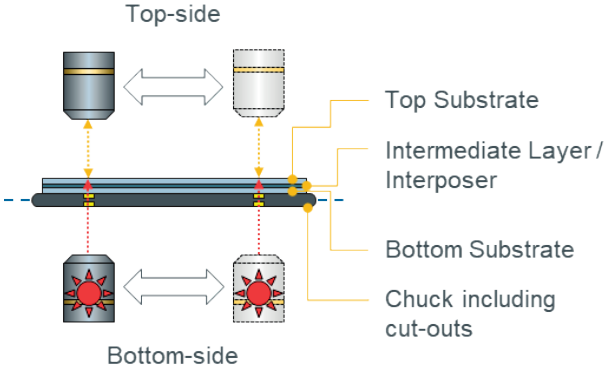

Figure 3 Schematic drawing of top and bottom-side alignment objectives

When considering the die distortion errors induced after reconstitution on the wafer, as is typical for FOWLP, the advanced distortion functionality should also be applied at the die level, where active compensation and re-routing results strictly rely on external metrology data. Distortion compensation algorithms include mathematical correction of rotation, scale, shear and translation (shift). For die-placement-error compensation, the model limits distortions within the dies to the rigid body of the die, which typically is represented by two (external) alignment points per die. Due to the immediacy of the conversion process, the dynamic binary pattern generation complements externally acquired metrology data of each die individually per substrate just before the exposure in order to compensate for overlay/positioning errors caused by handling or pre-processing excluding potential thermal influences. A simplified data integrity flow of die-level compensation is visualized on Figure 4.

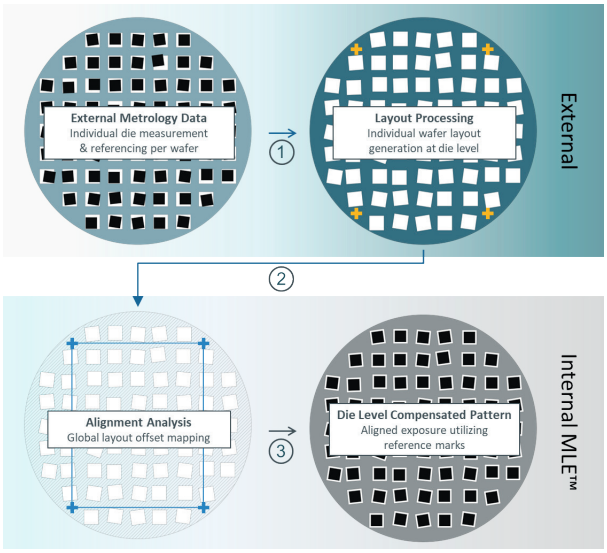

Figure 4
Die-level compensation schematic process flow

In parallel, MLE patterning enables real-time individualized wafer-level layouts as well as simultaneous structuring of individual die layouts; in particular, ad hoc die annotations, serial numbers, functional and directly readable encryption codes or active patterning of fuse maps to optimize device binning for process or device tracking and documentation, leading to improved overall yield. Additionally, programmable modulations of UV dosage at the sub-pixel level enable exposure gradients that lead to controlled resist-thickness-level variations after the development process, which is also known as greyscale lithography. This facilitates the fabrication of complex 3D multi-level resist patterns, which are applicable in multiple patterning processes, dual damascene, MEMS devices and micro-optical elements (e.g., refractive, diffractive). The digital programmable die/wafer layout can be stored in numerous industry layout design standard file formats (e.g. GDSII, Gerber, Oasis, ODB++, or BMP). Since the layout is computationally processed on the system under recipe control, neither resist type (positive/negative), exposure dose level, nor design layout complexity have any impact on the speed of the patterning process.

Patterning modularity and vital positioning in sub-grid

The resolution of MLE is aimed at typical back-end-of-line resolutions with fine control of the irradiated lines, as well as their gaps (L/S < 2 µm), while maintaining CD uniformity (CDU<10% CD) and positional accuracy of any arbitrary structures considerably in 248-nm patterning grid scale. This precision is matched by the distortion-free optics and the stage placement accuracy, which ensures seamless projection across the entire substrate. The exposure can be performed flexibly with a very high degree of freedom in intensity control as well as precise light-source-spectrum tuning to achieve optimal absorption and reliable processing for a wide range of commercially established as well as novel photoresists. The exposure light source operates at a wavelength spectrum of 375nm and 405nm, allowing for a mix and match of wavelengths to mimic known-good-process recipes (i.e. to follow the traditional mercury lamp spectrum) or to tailor the exposure towards specific customer demands. Both wavelengths can be simultaneously applied in any arbitrary mixture and thus enable thin-resist patterning, including positive, negative, polyimide, patternable dielectrics, dry film or even PCB materials and also support thick resist exposures at high aspect ratios typically encountered in wafer-level packaging, 3D MEMS patterning, microfluidics and integrated photonics applications. Figure 5 displays a series of SEM images of standard line-space resolution targets on 1 µm thick positive AZ MIR 701 resist on top, while results on bottom show line-space resolution tests on 2 µm thick negative tone resist AZ nLOF. In both cases, 1.5 µm L/S result was achieved through further process optimization involving the reduction of surface reflection effects, which can be achieved by applying anti-reflective coatings or modifying substrate material properties.

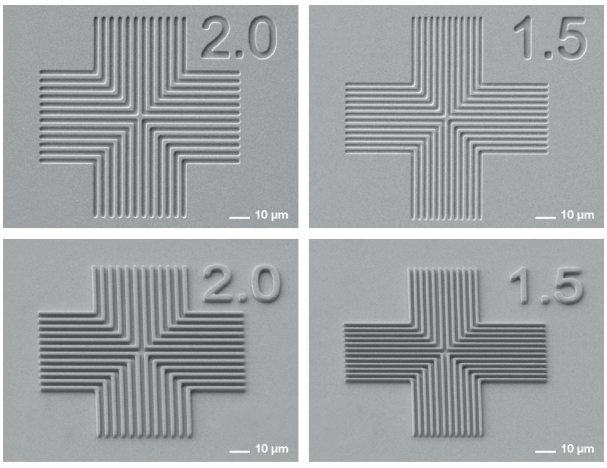

Figure 5
SEM results collage: Line space resolution tests on 1 µm thick positive AZ MIR 701 (top), Line space resolution tests on 2 µm thick negative AZ nLOF (bottom)

The MLE technology can also finely control depth of focus (DoF) in order to achieve steep sidewalls, and thus keep the desired 3D contour of the resist, or prevent edge topping and footing. Large working distance and automatic adaptive focus ensures patterning uniformity across the exposure surface. Commonly used TOK P-W1000T resist for fine-line and core-line RDL creation was chosen to demonstrate various lines and spacing patterning performance as well as sidewall patterning quality. Figure 6 shows examples of SEM images of baseline evaluation, demonstrating (A) 2 µm L/S resolution targeted on 8 µm film thickness, (B) 5 µm L/S resolution with meander pattern, (C) spacing variation of 1:2 ratio, and (D) L/S variation in both horizontal and vertical directions with ratios of 1:1, 1:2, 1:3, 1:4.

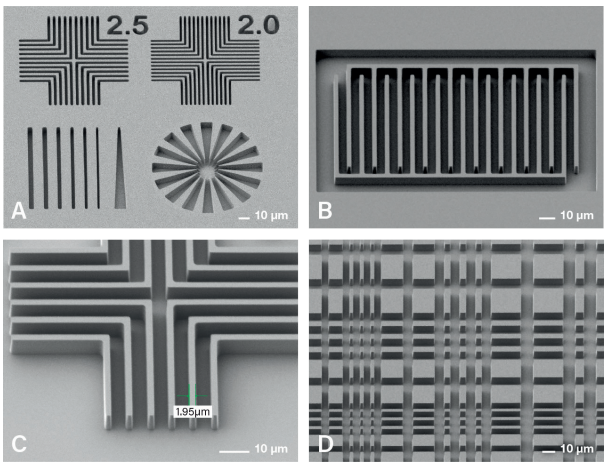

Figure 6
Baseline evaluation on (A) 8 µm thick TOK P-W1000T, (B) meander with 5 µm L/S, (C) 1:2 spacing variation, (D) L/S variation in both horizontal and vertical directions with ratios of 1:1, 1:2, 1:3, 1:4

Maskless operation scalability

Previously, back-end lithography results achieved during R&D using direct imaging equipment lacked the technological resilience for high-volume-manufacturing (HVM) lines equipped with steppers. Today, the industry sees increasing product mix, such as chiplets and segmented dies, as a driver for continued performance scaling, as well as variability of applications. This triggers the need for dynamic patterning at various resist thicknesses and dose levels. MLE provides a high DoF at 2 µm production resolution leveraging the physical diffraction limit established by the optics. At the same time, the scalability of MLE is broad in scope. The modular system scales according to user needs by adding UV exposure heads as shown in Figure 7 – for facilitating rapid transition from R&D to HVM mode, for throughput optimization, or for adaptation to different substrate sizes and materials – and is ideal for processing a range of substrates from small silicon or compound semiconductor wafers up to panel sizes.

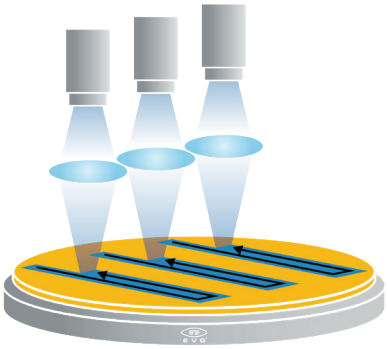

Figure 7
MLE's unique clustered exposure configuration enables exposure heads to be easily added to adjust for different throughput needs and substrate sizes

Summary

MLE provides a new approach for patterning through smart and agile digital processing while delivering unique maskless scalability in throughput and format with a consumables-free infrastructure. It achieves the same patterning performance regardless of photoresist thanks to a flexible, reliable and scalable high-power UV laser source combination featuring multiple wavelength options. The platform allows for patterning of a wide variety of materials such as silicon, mold, glass, polymers and laminates, using the same optics. The wafer chuck and autofocus system compensate for substrate bow and warp, which is especially important for applications like FOWLP. The almost unlimited design flexibility that the technology brings to the current conservative environment opens up room for new innovations, helps to shorten development cycles, and at the same time bridges the gap between R&D and HVM.

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