

## **Imec and EV Group demonstrate wafer-to-wafer hybrid bonding with 200nm interconnect pitch and record high overlay accuracy**

*Through their continued collaboration, Imec and EV Group (EVG) are focusing on advancing the overlay performance required for advanced logic-to-logic and memory-to-logic tier stacking*

- Imec and EV Group (EVG) demonstrate a highly yielding wafer-to-wafer hybrid bonding technology at 200nm Cu interconnect pad pitch with record high post-bonding alignment accuracy, obtained on a test vehicle with routable interconnects.
- This achievement marks a milestone in enabling advanced logic-to-logic and memory-to-logic tier stacking that requires an extremely high level of interconnect density – as envisioned in imec’s CMOS 2.0 scaling paradigm.
- The breakthrough result was achieved by co-optimizing all critical elements of imec’s wafer-to-wafer hybrid bonding process flow, and by leveraging EVG’s most advanced wafer bonding equipment.

**LEUVEN (Belgium), MAY 28, 2026**— This week, at the 2026 IEEE Electronic Components and Technology Conference (ECTC), imec, a world-leading research and innovation hub in advanced semiconductor technologies, and EV Group (EVG), leading provider of semiconductor manufacturing equipment and process solutions, present a robust and highly yielding wafer-to-wafer hybrid bonding technology at 200nm Cu interconnect pad pitch, demonstrated on a test vehicle with routable interconnects. In addition, a record high Cu pad alignment accuracy was achieved, leveraging EVG’s most advanced wafer bonding equipment. Imec and EVG intend to further advance the wafer-to-wafer hybrid bonding roadmap, in support of logic-to-logic and memory-to-logic tier stacking use cases that require an extremely high level of interconnect density – as envisioned in imec’s CMOS 2.0 scaling paradigm.

Future compute system architectures designed around imec’s CMOS 2.0 scaling paradigm are driving the wafer-to-wafer hybrid bonding roadmap toward 200nm interconnect pitch. With CMOS 2.0, a system-on-chip (SoC) is partitioned into heterogeneous, functional tiers that are reconnected using 3D interconnect technologies. Depending on the application, CMOS 2.0 envisions splitting the logic part of the SoC into a high-drive logic layer and a high-density logic layer. This logic-to-logic tier stacking requires extremely high interconnect densities, which can only be offered by the most advanced wafer-to-wafer hybrid bonding technology.

Imec now demonstrates a robust wafer-to-wafer hybrid bonding technology at 200nm interconnect pitch, obtained on a test vehicle with four layers of routable interconnects pre-processed on each of the wafers prior to bonding. In addition, a Cu pad-to-pad post-bond overlay vector below 40nm was obtained for 100% of the dies over the full 300mm wafer – a world first. EVG’s cutting-edge hybrid and fusion wafer bonding system, the GEMINI® FB, was essential for achieving this unprecedented overlay accuracy – critical for ensuring a high electrical yield.

Zsolt Tokei, imec fellow and program director of 3D system integration: “This breakthrough fine-pitch hybrid bonding result was achieved by co-optimizing all the critical elements of imec’s hybrid bonding

process flow. These include, among others, the use of SiCN as the dielectric material (as pioneered by imec) and a chemical mechanical polishing (CMP) step prior to bonding. The latter was optimized for high across-wafer uniformity to produce extremely flat dielectric surfaces while achieving a controlled few nanometers of recess for the Cu pads. The high overlay accuracy and control, enabled by EVG's wafer bonding tool, were additionally facilitated by an improved Cu pad design and by pre-bond lithography corrections."

"We continue to advance our hybrid wafer bonding flow and drive the roadmap well below 200nm interconnect pitch to unlock the most demanding logic-to-logic and memory-to-logic stacking use cases," adds Zsolt Tokei. "This will require even more enhanced overlay performance, which we intend to further explore in collaboration with EVG."

"The long-standing collaboration with imec reflects the important role that wafer bonding continues to play in enabling next-generation semiconductor devices," stated Paul Lindner, executive technology director at EV Group. "Over more than three decades of working together, we have demonstrated how close collaboration between equipment suppliers and leading research organizations such as imec can drive meaningful advances in process technology. We look forward to continuing this work to support future device architectures and to strengthen collaboration across the global semiconductor ecosystem."

The presented wafer-to-wafer hybrid bonding results are detailed in the 2026 ECTC presentation: 'Wafer-to-wafer hybrid bonding technology with 200nm interconnect pitch,' S. Van Huylbroeck *et al.* (Session 26: Advanced Wafer-to-Wafer Hybrid Bonding – Fri., May 29, 10:10am).

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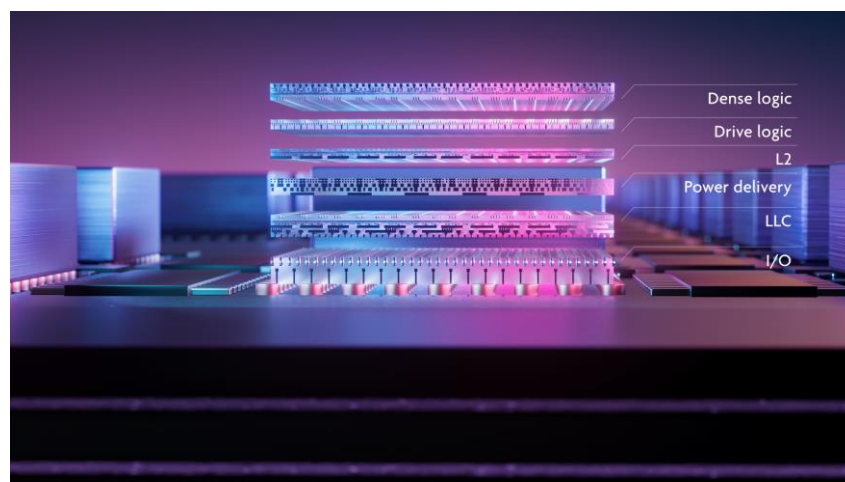


Figure 1: Example of a possible partitioning of a SoC following imec's CMOS 2.0 scaling paradigm. (credit: imec)

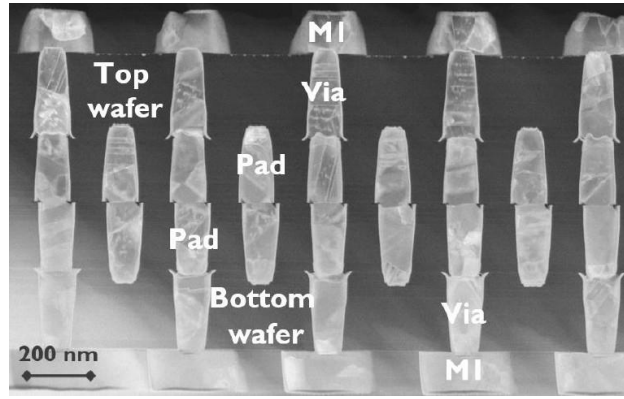


Figure 2 – TEM of Daisy chain structures on a 200nm hexagonal pad grid with equal hybrid pad size and 25% designed Cu density. (credit: imec/IEEE)

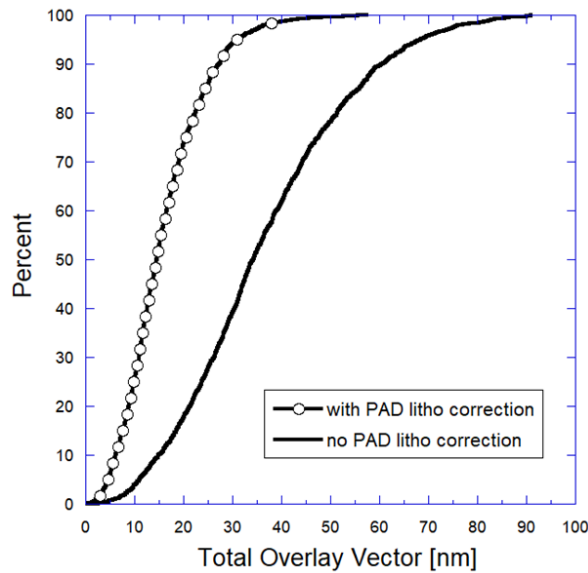


Figure 3 – Actual wafer-to-wafer bond alignment improvement obtained on electrical device wafers. Results are shown with and without applying hybrid pad lithography pre-bonding corrections. (credit: imec/IEEE)

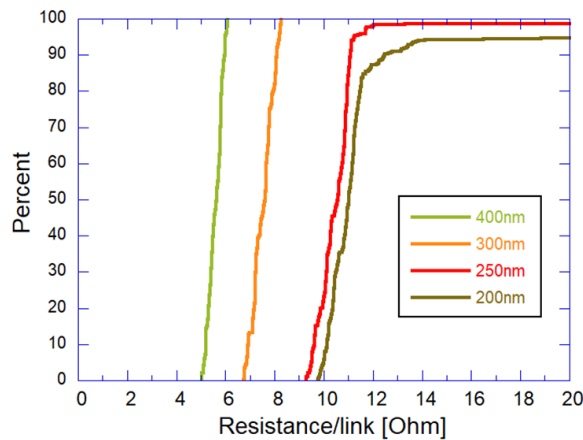


Figure 4 – Cumulative plot of the measured resistance per link for equal pad size structures with 25% Cu density. (credit: imec/IEEE)

## About imec

Imec is a world-leading research and innovation hub in advanced semiconductor technologies. Leveraging its state-of-the-art R&D infrastructure and the expertise of over 6,500 employees, imec drives innovation in semiconductor and system scaling, artificial intelligence, silicon photonics, connectivity, and sensing.

Imec's advanced research powers breakthroughs across a wide range of industries, including computing, health, automotive, industry, consumer electronics, aerospace and security. Through IC-Link, imec guides companies through every step of the chip journey - from initial concept to full-scale manufacturing - delivering customized solutions tailored to meet the most advanced design and production needs.

Imec collaborates with global leaders across the semiconductor value chain, as well as with technology companies, start-ups, academia, and research institutions in Flanders and worldwide. Headquartered in Leuven, Belgium, imec has research facilities in Belgium, across Europe, the USA and the GCC region, and representation on three continents. In 2025, imec reported revenues of €1.2 billion. For more information, visit [www.imec-int.com](http://www.imec-int.com)

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## About EV Group (EVG)

EV Group (EVG) provides innovative process solutions and expertise that serve leading-edge and future semiconductor designs and chip integration schemes. The company's vision of being the first in exploring new techniques and supporting next-generation applications of micro- and nanofabrication technologies enables customers to successfully commercialize new product ideas. EVG's high-volume-manufacturing-ready products, which include wafer bonding, lithography, thin-wafer processing and metrology equipment, enable advances in semiconductor front-end scaling, 3D integration and advanced packaging, as well as in other electronics and photonics applications.

More information about EVG is available at [www.evgroup.com](http://www.evgroup.com)

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